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Research and Development Technical Report
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MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

2ND QUARTERLY REPORT

By

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JANUARY 1977

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US ARMY ELECTRONICS COMMAND • FORT MONMOUTH, NEW JERSEY 07703

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MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH POWER BULK SEMICONDUCTOR LIMITERS

SECOND QUARTERLY REPORT

23 September 1976 to 22 December 1976

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The objective of this Manufacturing Methods and Technology Engineering Program is to establish the producibility of the X-band semiconductor bulk limiter and the X-band bulk semiconductor - lower power diode multistage limiter by mass production techniques. During the quarter, X-band semiconductor bulk limiters with power handling capability of 20-30kW were fabricated from new high resistivity silicon and were characterized for their RF performance along with multistage clean up limiter. Two (2) bulk limiter elements were →

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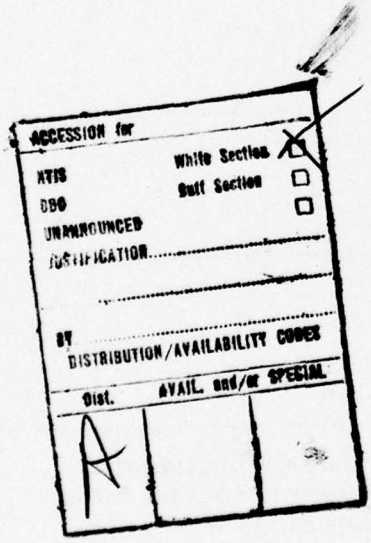
ABSTRACT (continued)

mounted in a dual slot X-band iris to provide increased bandwidth. A new microwave circuit was implemented to provide the required operating bandwidth for the combined bulk limiter and diode clean up limiter stages.



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PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U. S. Army Electronics Command Technical requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G, and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No., 15, dated December 1975, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III, and IV a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually,

any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVE

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486 are summarized below.

A. Function Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a common semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight:	7.0 oz max
Input Flange:	mates with UG-40B/U choke flange
Output Flange·	mates with UG-135/U cover flange
Mounting Position:	any
Cooling:	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF input power:	30 kW, Du = .001
1μsec pulses continuous:	10 kW, Du = .01
Insertion loss:	0.7 dB (max)
Low level VSWR:	1.4:1 (max)
Recovery time:	0.8 μsec (max)
Flat leakage:	50 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
Spike leakage:	750 mW (max), for 30 kW, .001 duty cycle, 1 μsec pulse
External bias:	none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P		30	kW
Average Power	P_a		100	W
Ambient Temp.	T_A	-55	+85	^oC
Altitude	--		50,000	ft

II. INTRODUCTION

This report covers the period from 23 September 1976 through 22 December 1976. During the period, high-power bulk semiconductor limiter work was concentrated in the areas of semiconductor wafer fabrication, broadband matching circuitry and increasing the bandwidth of the high-power bulk limiter stage.

Difficulties had been encountered during the first quarter in diffusing limiter chips which had low impedance DC current-voltage characteristics. Microwave limiters fabricated from these elements showed premature burn-out at power levels of only a few kilowatts. During the second quarter, techniques to improve wafer fabrication were introduced which included polishing the wafers to near final thickness to improve wafer flatness, performing photolithography process on unmounted wafers, and using boron nitride source wafers for the boron diffusion process. By the end of the second quarter a number of wafers had been produced which had low impedance current-voltage characteristics.

Earlier test results on the bulk limiter-diode limiter package structure had shown a reduced power handling capability as a result of tuning screws placed in front of and behind the bulk semiconductor limiter. A theoretical analysis was performed to determine the interaction between broadband tuning techniques and the power handling capability of the packaged limiter. The theoretical results were combined with experimental circuit testing to develop a structure in which the bulk limiter is the input stage to a bandpass filter structure. The second engineering samples have been constructed using the new circuit and show considerable improvement in performance over the first engineering samples.

From the circuit tests of the three-stage limiter package, it was determined that the input bulk stage would require a 3 dB bandwidth of over

1.32 GHz and a power handling capability of 30 kilowatts in order to achieve the program goals. Further, our analysis indicates that this can not be achieved with a single 3 mil thick limiter element. Consequently, bulk limiters were made using two elements, one in each slot of double slot limiter irises. These limiters showed good limiting performance and more than adequate bandwidth. However, a problem was encountered in that burnout could not be predicted from recovery time measurements as was possible with single slot limiters. We are currently examining an alternate circuit using two bulk limiter elements mounted in series in the same slot as a solution to this problem.

The subsequent sections of this report describe in greater detail the work performed and results achieved to date. Also included are conclusions based on the work and program plans for the third quarter.

III. BULK SEMICONDUCTOR CIRCUIT TUNING ANALYSIS

A. Introduction

The bulk semiconductor limiter element is a high impedance microwave device which has an electrical conductivity which is a function of the microwave voltage across the device. The circuit with which the element is used must meet certain requirements to yield optimum low and high power microwave performance. For example, incident low level microwave power absorbed by the device contributes to insertion loss. The percentage of low level power absorbed by the device can be easily reduced by lowering the circuit impedance at the limiter element terminals. Note that for any given limiter element that lowering circuit impedance would also widen the bandwidth substantially as the capacitive susceptance of the limiter element would have a smaller effect in the lower impedance circuit. Thus, lowering the circuit impedance presented across the limiter element terminals improves the low level characteristics of the completed component.

An examination of the high power isolation state of the limiter device shows that lowering the circuit impedance at the element terminals reduces the isolation which results from a given element conductance. The reduction in isolation results in an increase in dissipated power within the device and consequently reduced power handling capability and increased return loss. Thus, lowering the impedance at the element terminals degrades all high power performance characteristics.

As a consequence, it is necessary to select the transmission line impedance presented to the limiter element terminals at a compromise value which provides both optimum high level and low level performance. Further, in designing tuning circuits to provide for broadband low level characteristics, it must be remembered that high power performance will be

affected by the choice of that design. For optimum performance over the band of operation a frequency independent impedance at the element terminals is desired.

B. Example

To illustrate the effects of the impedance at the plane of the limiter element, consider the case of the bulk limiter design shown in Fig. 1a. The design has been simplified by eliminating the turns ratio and transforming the reactance values to a normalized 1 ohm transmission line.

If we assume that the element has two values of resistance, a maximum of 17.12 ohms in the low power state and a minimum of 0.03 ohms in the high power state, we can calculate the following performance parameters for the limiter circuit:

Circuit (1a) Low Power ($R_T = 17.12\,\Omega$)

$f_o = 9.32$ GHz

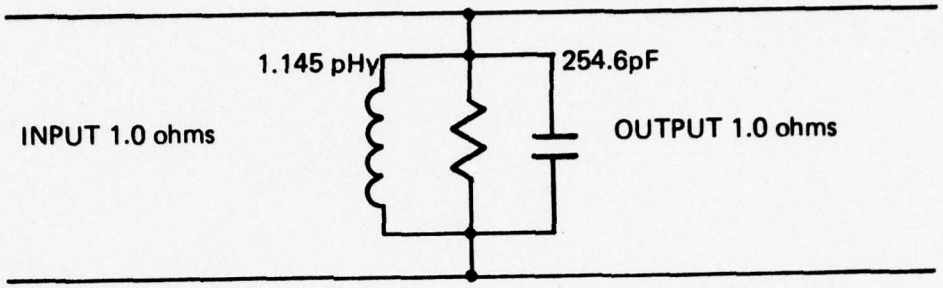
BW (3 dB) = 1.25 GHz

IL = 0.25 dB

Circuit (1a) High Power ($R_I = 0.03\,\Omega$)

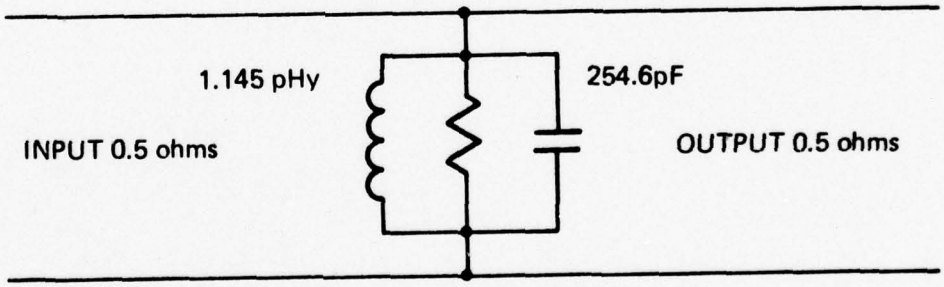
Isolation = 24.9 dB

Fractional Power Dissipated $\frac{P_d}{P_i} = 0.107$



R_T = 17.12 ohms (0.25 dB)
R_I = 0. 03 ohms (24.9 dB)

a) NORMALIZED TO 1.0 OHM



R_T and R_I as above

b) IN REDUCED IMPEDANCE LINE

FIGURE 1 BULK LIMITER EQUIVALENT CIRCUIT

The relationships:

$$\frac{P_i}{P_t} = \left| 1 + \frac{Y_x Z_o}{2} \right|^2$$

and

$$\frac{P_d}{P_i} = \frac{Z_o G_x}{\left| 1 + \frac{Y_x Z_o}{2} \right|^2}$$

are used to calculate all of the above parameters.

Now, assume that the transmission line has a lower impedance in the plane of the limiter element caused by the matching circuitry used. The impedance of the circuit shown in 1b is reduced by a factor of two to a value of 0.5 ohms. Again calculating the low and high power performance of the limiter circuit yields:

Circuit (1b) Low Power (R_T = 17.12 Ω)

f_o = 9.32 GHz

BW (3 dB) - 2.5 GHz

IL = 0.13 dB

Circuit (1b) High Power (R_I = 0.03 Ω)

Isolation = 19.4 dB

Fractional Power Dissipated $\frac{P_d}{P_i}$ = 0.191

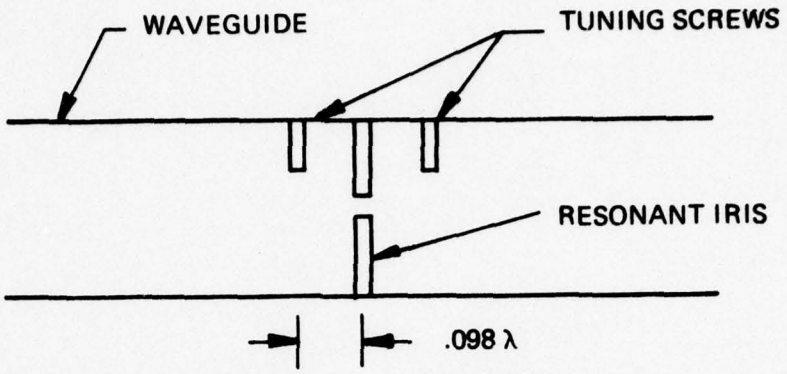
Thus, while the circuit of Fig. 1b improved low power performance greatly by minimizing the insertion loss and broadening the bandwidth of the device, it did so only at the expense of high power performance. The isolation was reduced from 24.9 dB to 19.4 dB and the power absorbed by the device from the incident microwave pulse increased by a factor of 1.79. Thus, the power handling capability of the device was reduced by a similar factor.

The above example was given to illustrate that the impedance presented by the circuit to the limiter element terminals is extremely important in its effects on device operation and power handling capability. A bulk limiter element will be capable of dissipating a fixed amount of energy during a high power microwave pulse. Therefore, in order to maintain both good high and low power performance characteristics, the matching circuity used to couple the bulk semiconductor stage to the lower power stages must be well understood.

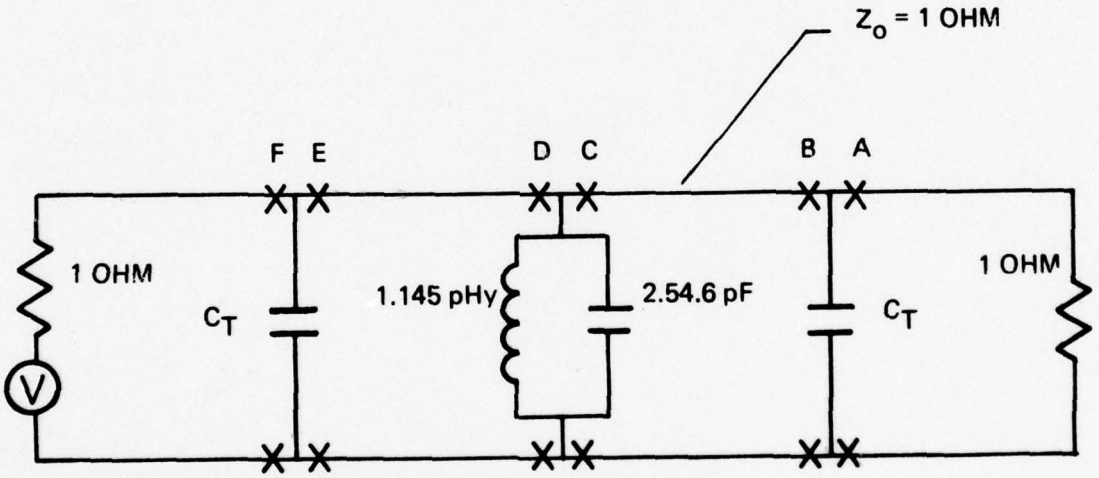
C. Capacitive Tuning

Now examine the effect of using symmetrical capacitive tuning arrangement on either side of the bulk limiter. Figure 2a shows the geometrical arrangement of tuning screws which will successfully match present bulk limiters to the low level PIN stages at low power levels. Figure 2b is an equivalent circuit of the above structure with the waveguide impedance and limiter element values normalized to 1 ohm. C_T represents the capacitance of the tuning screws in the transmission line.

The object is to match the power from the one ohm input port to the load resistor over the frequency band of interest. For the sake of simplicity we can analyze the transmission state with $R = \infty$, the lossless case. From transmission line theory it is known that if one divides the transmission line at any point, the impedance of the portion looking toward



a) PHYSICAL CIRCUIT



b) EQUIVALENT CIRCUIT

FIGURE 2 CAPACITIVE TUNED BULK LIMITER

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the source must equal the complex conjugate of the impedance of the portion looking toward the load for maximum power transfer to occur. Thus, if a matched transmission line circuit were cut and the impedance of the load portion were measured at

$$Z_L = 0.7 + j\,0.5\,\Omega$$

then it follows that the impedance of the source portion would be

$$Z_S = 0.7 - j\,0.5\,\Omega$$

Similarly, if a symmetric circuit were divided at the center it follows that for a matched condition to exist the impedance of both halves would necessarily be real and equal.

This leads to the analysis of the circuit of Fig. 2b at 9.32 GHz. The Smith chart of Fig. 3 shows the impedance of the circuit calculated from the load end. Assume a susceptance value of $+j\,0.7$ has been used for C_T. Point A is the impedance of the 1 ohm load and transmission line. Point B includes the susceptance of the load side capacitor C_T. At Point B the impedance of the circuit looking toward the load is $Z_B = .67 - j\,.47$ ohms. As we move back toward the generator by approximately 1/10 wavelength, Point C, we find the impedance to be entirely real with a value of 0.5 ohms. At resonance, 9.32 GHz, the limiter circuit appears as an open circuit (lossless case) and the impedance at Point D is the same as that at Point C. Moving back another 1/10 wavelength yields a load impedance from Point E of $Z_E = .67 + j\,.47$. This inductive component is cancelled out by the generator side susceptance of $C_T = j\,0.7$ mhos yielding a load side impedance of 1.0 ohms at Point F. Analysis of the same circuit at the band edges of 9.0 and 9.65 GHz yields the following results:

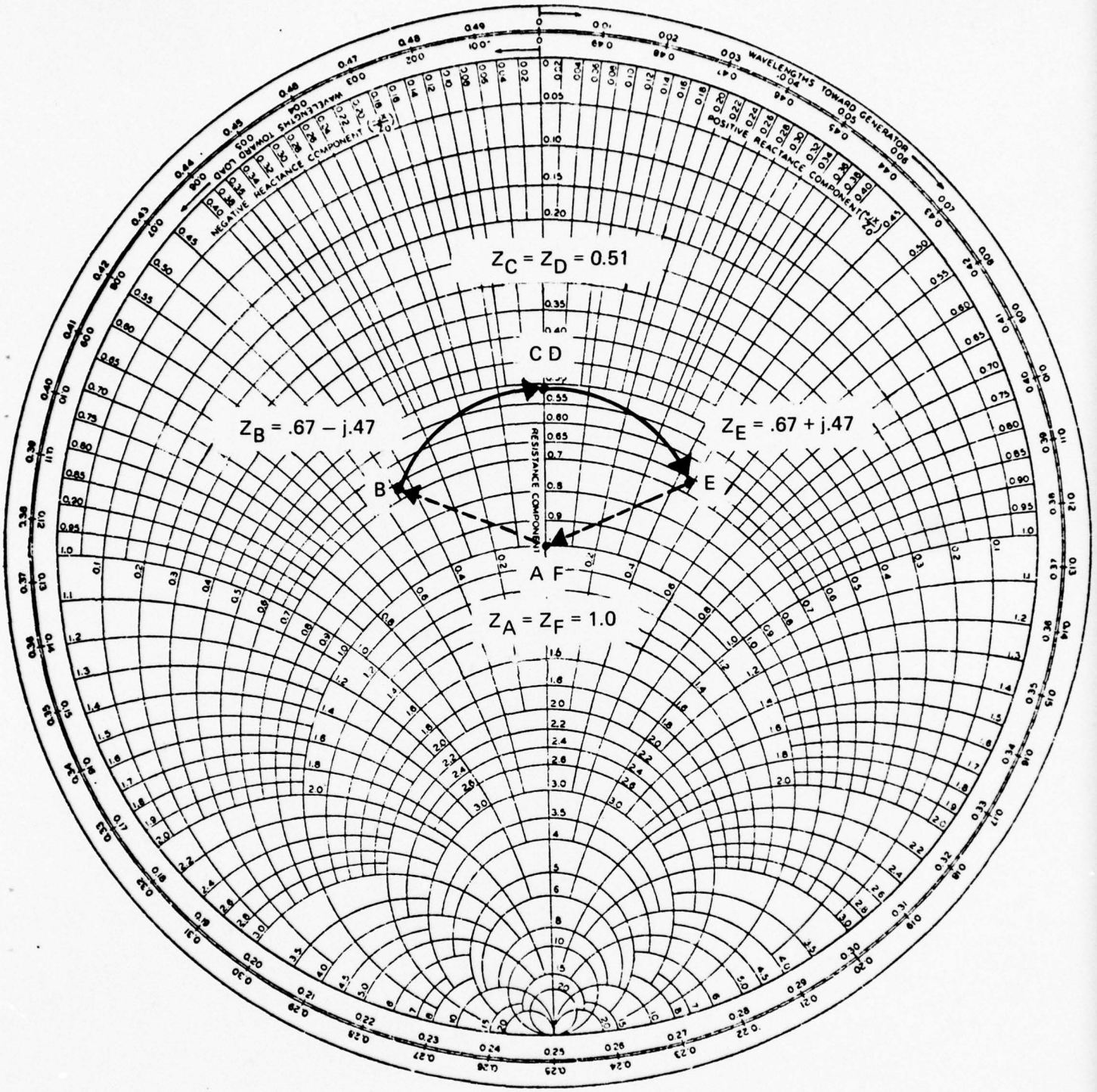

FIGURE 3 IMPEDANCE PLANE ANALYSIS OF CAPACITIVE TUNED BULK LIMITER

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Without Tuning:

f_o	S_{11}	IL
9.0 GHz	$0.46 \angle -63^\circ$	1.04 dB
9.32 GHz	$0 \angle 0^\circ$	0.0 dB
9.65 GHz	$0.46 \angle +63^\circ$	1.04 dB

With Tuning Capacitors spaced 0.098 λ at 9.32 GHz, B = 0.7 mhos at 9.32 GHz

9.06 GHz	$0.24 \angle 179^\circ$	0.26 dB
9.32 GHz	$0^\circ \angle 0^\circ$	0.0 dB
9.65 GHz	$0.22 \angle -38^\circ$	0.21 dB

In performing the analyses the following impedances were noted as a function of frequency at the iris plane (Point C in Fig. 2a):

Frequency	Admittance	Impedance
9.0 GHz	1.91 + j .06	0.523 - j .016
9.32 GHz	1.98 + j 0	0.505 + j 0
9.65 GHz	2.03 - j .1	0.491 + j .012

Thus, it is seen that the effect of the two tuning capacitors of Fig. 2a is primarily to lower the circuit impedance at the plane of the resonant limiter iris. Very little reactive tuning occurs because the capacitors do not present a rapidly varying susceptance at the window plane.

D. Wide Space Capacitive Tuning

Very broadband tuning can be provided for the iris limiter circuit, however, by using capacitors spaced far apart on the waveguide transmission line. For example, the circuit shown in Fig. 4 will have very broad characteristics with considerably less reduction in iris plane impedance than found with the circuit of Fig. 2b. However, the dimensions of the circuit

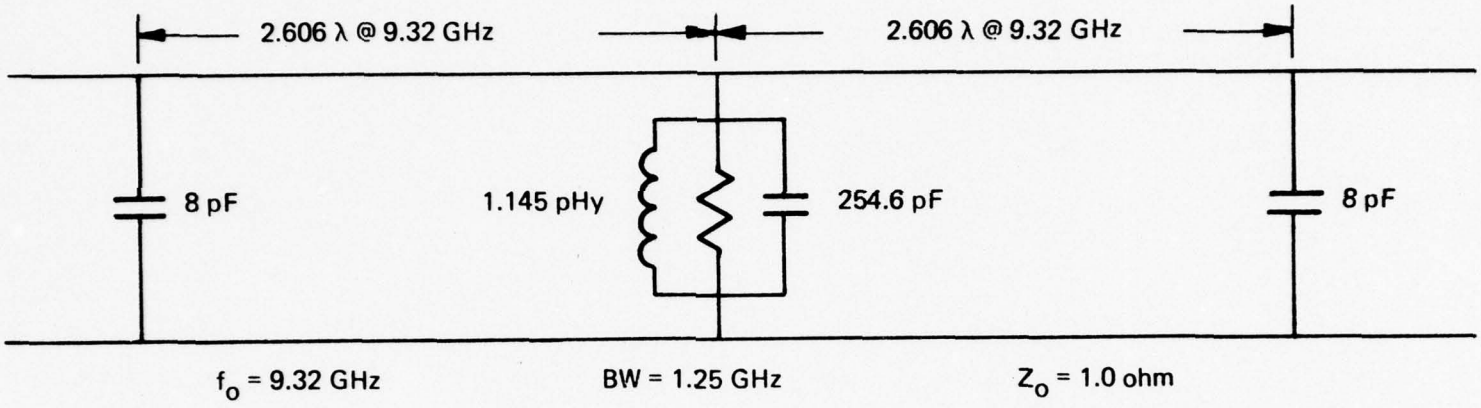


FIGURE 4 BULK LIMITER BROADBAND TUNED WITH WIDE SPACED CAPACITORS

are too large to be implemented and it therefore need not be considered further.

E. Circuits for Consideration

It has been shown that waveguide tuning circuits which do not present rapidly varying reactance at the limiter element plane can only improve low level performance by reducing the resistive impedance component at the limiter element plane. This deteriorates the high level performance severely. Hence, only circuits with long spacial dimensions or rapidly varying reactance versus frequency characteristics will be capable of providing the desired performance.

Circuits capable of providing the desired performance are shown in Fig. 5. Both circuits will show a midband frequency shift either upward (for spacings of approximately 0.17 λ) or downward (for spacings of approximately 0.33 λ). One of these two circuits or a variation thereof will have to be used for achieving broadband performance from the bulk limiter in a short length of waveguide.

Analysis of the two circuits shown in Fig. 5 produces the conclusion that circuit 5b, the double tuning circuit, will provide the best limiting performance. Figure 6 shows a complete analysis of circuit 5b using the following circuit parameters:

Limiter Iris Parameters

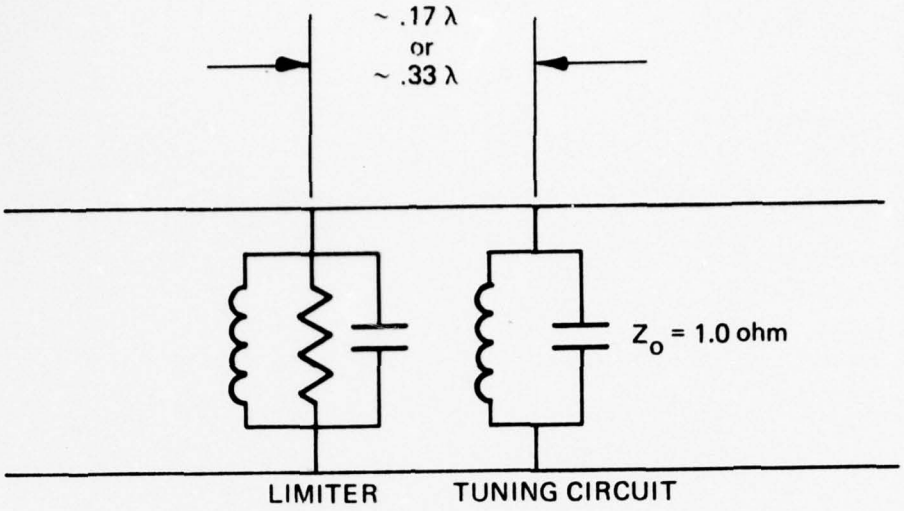
f_o = 9.15 GHz

BW (3 dB) = 1.25 GHz

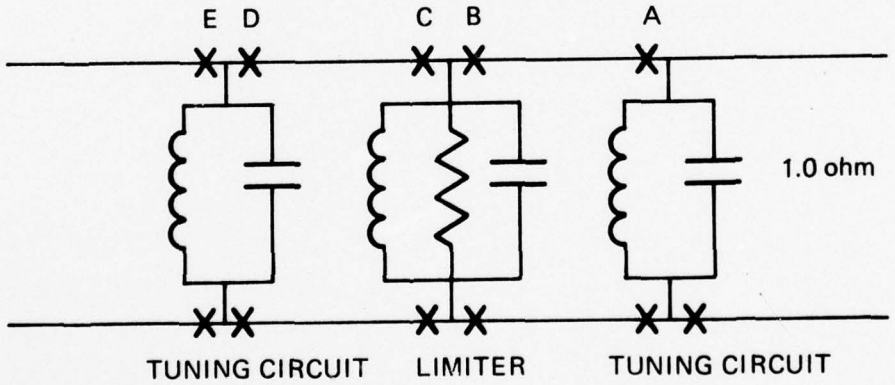
R = ∞ (lossless case)

C = 254.6 pF

L = 1.88 pHy



a) SINGLE TUNING CIRCUIT DESIGN



b) DOUBLE TUNING CIRCUIT DESIGN

FIGURE 5 RESONANT CIRCUIT BROADBAND TUNING OF BULK SEMICONDUCTOR LIMITERS

Tuning Iris Parameters

f_o = 9.15 GHz

BW (3 dB) = 2.50 GHz

C = 127.3 pF

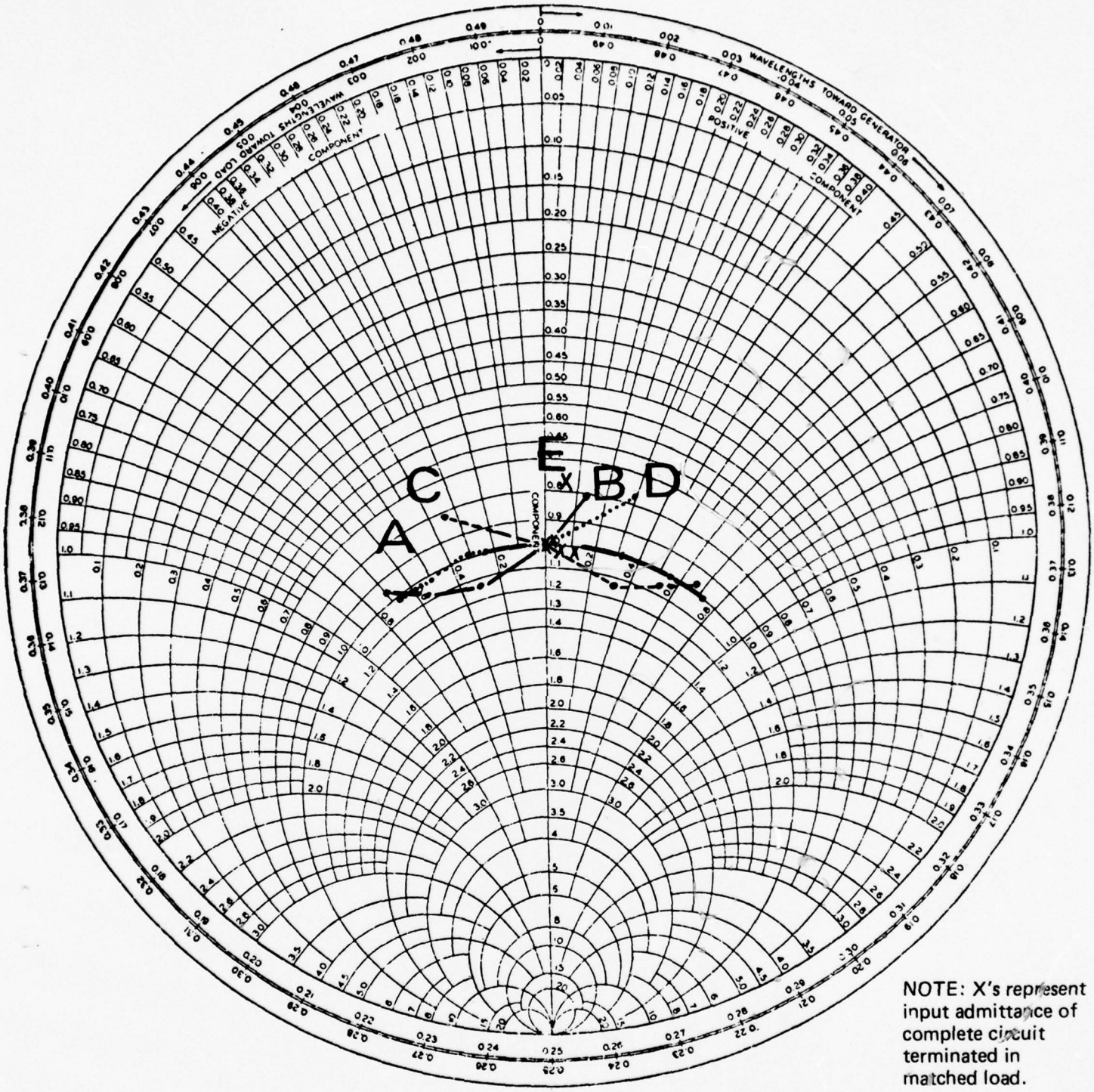
L = 2.376 pHy

Tuning Iris to Limiter Spacing

Spacing = .191 λ at 9.15 GHz

The analysis was carried out at five frequencies within the operating bandwidth 9.0, 9.15, 9.35, 9.5, and 9.65 GHz. The curves on the admittance plane plot (Fig. 6) represent the various lettered points on the circuit diagram (Fig. 5b) as a function of frequency. All curves are labeled at their low frequency end and the 9.15 GHz point on all curves is coincident with the origin. The input admittance to the circuit (plane E admittance) is shown by points labeled X on the Smith chart.

It is important to note two factors in this analysis. First, very good matching was obtained over the 9.0 GHz to 9.65 GHz frequency range of interest. The magnitude of S_{11} is less than 0.14 for all frequencies. This corresponds to a return loss of greater than 17 dB which more than meets the VSWR specification of 1.4:1. Second, the impedance at the limiter element plane does not vary too much with frequency. This can be seen by reading the conductance value off of either curve B or C as a function of frequency. Minimum conductance is 0.78 mhos; maximum is about 1.13 mhos. Thus, the impedance variation is 1.45 to 1. Careful examination of the Smith chart shows that this can be reduced still further by a slightly wider spacing of the tuning elements.



NOTE: X's represent input admittance of complete circuit terminated in matched load.

FIGURE 6 ADMITTANCE PLANE ANALYSIS OF CIRCUIT 5b

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F. Recommended Circuit Configuration for Multi-Stage Limiter

It is recommended that the left portion of the circuit Fig. 5b be the tuning design for the multi-stage limiter component, Thus, the circuit should consist of:

1. An input pressure window resonant at 9.1 - 9.15 GHz with a bandwidth of twice the limiter bandwidth.
2. A section of waveguide transmission line approximately 0.19 wavelengths long at the iris f_o.
3. The bulk limiter stage (minimum bandwidth approximately 1.35 GHz).

The remaining reactive tuning, supplied at Plane A in Fig. 5b, can be supplied by the low level limiter stage provided that the spacing between the bulk limiter and the low level stage has the proper value.

It is very important to note that as long as the circuit to the left of the bulk limiter contains only those components and spacings specified, no tuning element placed on the right of the bulk limiter will affect power handling capability adversely. Thus, tuning screws and the like can be used as desired to obtain low frequency performance.

G. Test of Three Stage Filter Design

A three stage filter design was analyzed at RRC for achieving the necessary tuning. The bulk limiter stage was assumed to have the following characteristics of frequency and bandwidth.

f_o = 9.15 GHz

BW (3dB) = 1.25 GHz

These values were based, in part, on the results of the first engineering samples. The 1.25 GHz bandwidth should be obtainable simultaneously with a 30 kW power capability if two bulk limiter elements are used in either a double or single slot iris.

Two passive irises with the same center frequency, 9.15 GHz, and twice the 3 dB bandwidth or 2.5 GHz were used in the design. The completed filter structure has a passive tuning iris, the active bulk semiconductor limiter, and a second passive tuning iris all separated by 0.19 wavelength spaces. The theoretical analysis indicated a bandwidth considerably in excess of the needed 650 MHz. Further, the analysis showed minimal impedance variation of the limiter plane as a function of frequency. Hence, good performance was anticipated.

Unfortunately, in high power testing the circuit it was found that the electric field across the input tuning iris was very high and arcing occurred during high power testing. Thus without development of a tuning resonator capable of withstanding the high power pulses without arcing, this circuit cannot be used.

In order to evaluate the effectiveness of the three stage tuning mechanism a test was run at RRC to optimize the structure for input VSWR. The test included a two stage diode limiter similar to MA 3940X as part of the structure. No tuning screws were used to optimize the structure, as tuning screws in front of the bulk limiter will reduce the impedance at the limiter. The overall mechanical arrangement is as shown in Fig. 7, as are the parameters of the three resonant irises used in the experiment. The result of the test was a return loss of 16 dB or greater over the frequency range of 9.080 to 9.805 GHz or a 1.38:1 VSWR over a 725 MHz bandwidth. The insertion loss varied from 0.9 dB at the bottom of the passband to 0.7 dB over the rest of the operating bandwidth.

IRIS PARAMETERS

IRIS	f_o	BW (3 dB)	IL
B3	9.28 GHz	1.21 GHz	0.25 dB
B5	9.30	2.44	0.05
B6	9.30	2.37	0.05

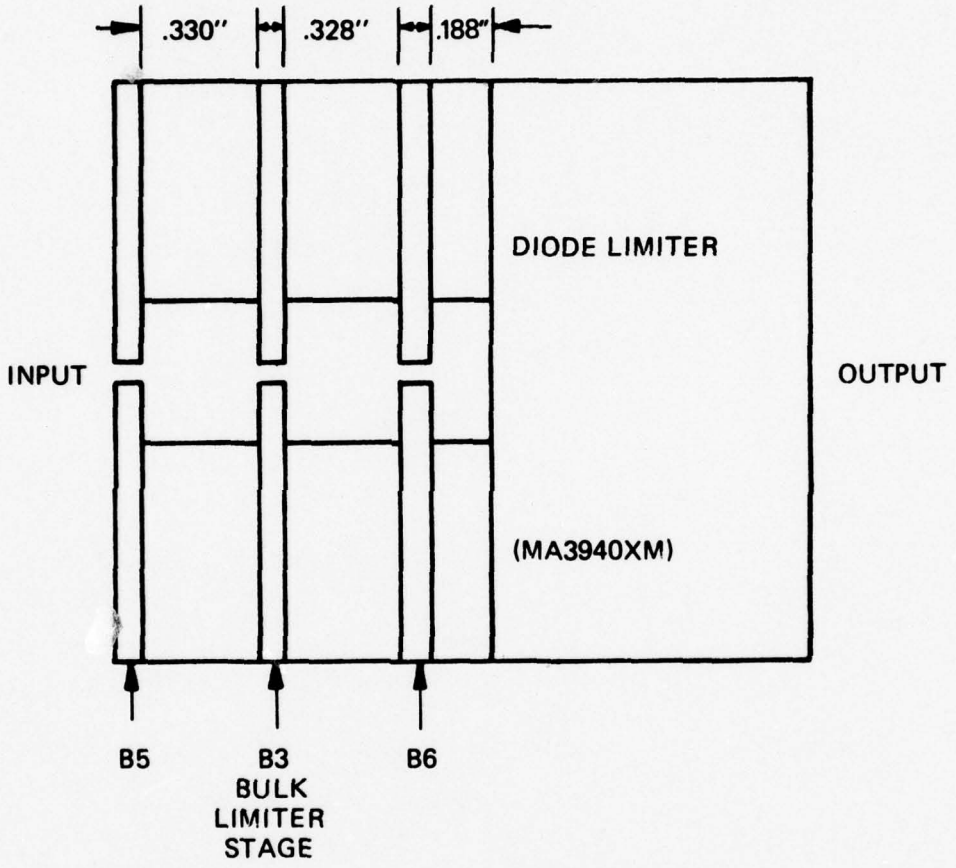

FIGURE 7 THREE STAGE FILTER TEST

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Thus, the three stage filter in front of the diode limiter is capable of providing the necessary tuning. However, we cannot implement it without first coming up with a tuning iris that can withstand the high fields caused by the reflected power under high power conditions.

H. Alternate Filter Design

Thus, it is necessary to examine filter structures which do not require an input filter element in front of the bulk semiconductor limiter. The bulk semiconductor limiter becomes conductive under high power conditions. Therefore, it does not arc because the electric field is greatly reduced by the shunt conductance at the iris plane. Tuning elements located on the low power side of the bulk limiter are never exposed to high values of electric field because of the shorting action of the bulk limiter. Therefore, any design which utilizes the bulk limiter itself as the input stage will not require high power tuning elements. It should also be noted that no impedance transformation can occur if the bulk limiter is the input stage of the filter structure. Thus, the power handling, insertion loss and recovery characteristics of the bulk limiter should be essentially independent of frequency.

An analysis of a simple two element filter using identical resonant irises spaced apart by a section of waveguide was performed. Based on geometrical Smith chart observations two spacings were examined, 0.25 wavelengths and 0.186 wavelengths. The conclusion was reached that using lossless resonant irises with resonant frequencies of 9.15 GHz and 3 dB bandwidths of 1.25 GHz, the maximum 1.4:1 VSWR bandwidth occurs at a spacing of 0.186 wavelength and is approximately 445 MHz. This result did not include possible tuning effects of the diode limiter stage which were difficult to incorporate in the analysis. It was therefore decided to conduct a set of experimental tests to evaluate the performance to be expected.

I. Limiter Input Filter Results

Considerable experimentation was performed with the bulk limiter stage (a dummy iris with known center frequency, bandwidth, and insertion loss) as the input stage of the filter. The best result was obtained with the tuning structure including the MA 3940XM diode limiter stage shown in Fig. 8. The diode limiter was adjusted to provide the maximum 1.4:1 VSWR bandwidth as was the tuning screw shown in the figure. The best result obtained was a passband from 9.045 GHz to 9.634 GHz or a 589 MHz bandwidth. This is slightly less than the 650 MHz desired, but indicates that the circuit is nonetheless useable. It is anticipated that adequate performance could be realized if the bandwidths of irises B4 and B3 were greater by 15 to 20%.

It is therefore concluded from the experimental results of the low power filter testing that a limiter input filter as shown in Fig.8 will yield the desired 650 MHz passband provided that the 3 dB bandwidth of the high power limiter stage is 1.32 GHz or greater. It should be understood that any tuning mechanism used on the low power side of the bulk limiter will neither be required to withstand high levels of microwave power nor reduce the impedance at the limiter plane at any frequency. Hence the power capability of the bulk stage will not be affected by the tuning or low level stage.

It is also worth noting that the diode clean up limiter does not have the optimum reactive tuning characteristics to broadband the two stage bulk semiconductor limiter. It is a wide bandwidth structure designed to have a flat passband. Therefore, it cannot present a matching reactance to the bulk limiter tuning iris circuit in the middle of the operating bandwidth.

Observations of the tuning interaction between the bulk limiter tuning iris stage and the diode limiter stage indicate that the reactance of the diode limiter stage interacts with that of the bulk limiter stage at one of

IRIS PARAMETERS

IRIS	f_o (GHz)	BW (3 dB) (GHz)	IE (dB)
B4	9.29	1.15	0.20
B3	9.28	1.21	0.25

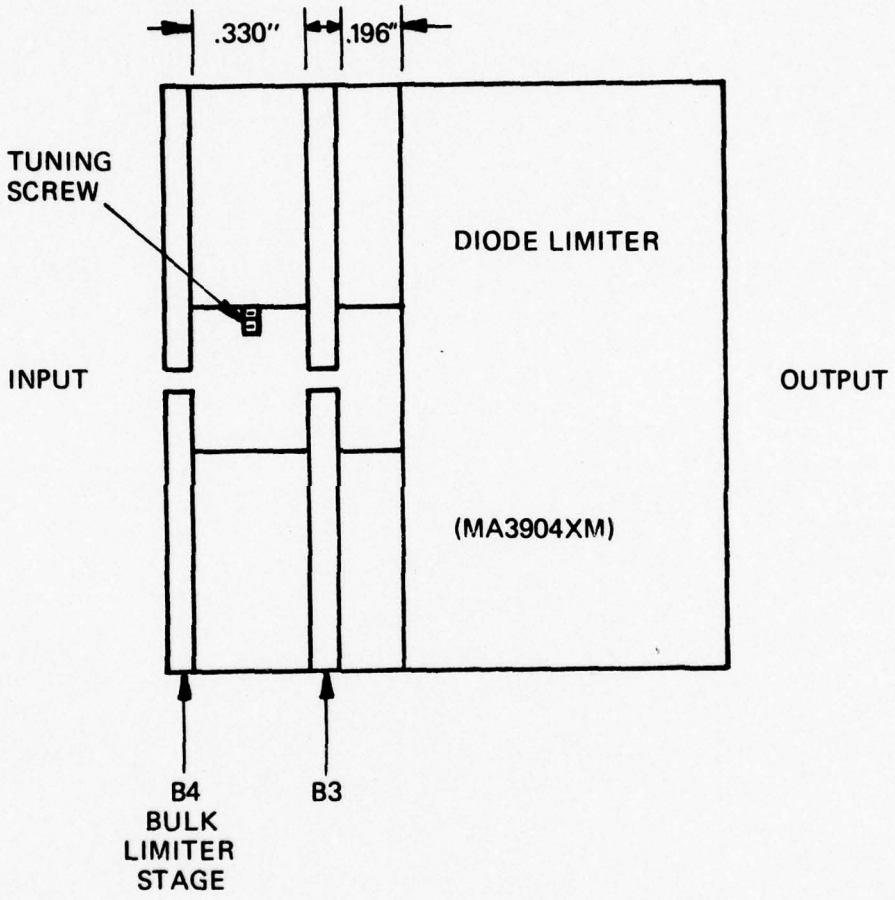


FIGURE 8 TWO STAGE FILTER EXPERIMENTAL TEST

the two band edges. The spacing of the bulk limiter and tuning iris must be such that the VSWR does not exceed the 1.4:1 specification at the filter's center frequency when tested alone. The parameters of the diode limiter can then be adjusted in the assembled package to broaden the passband on either the low or high frequency end. The return loss characteristic observed for the tuned structure of Fig. 8 is shown in Fig. 9. There are three minima in the return loss characteristic within the 589 MHz bandwidth defined by the 1.4:1 return loss specification.

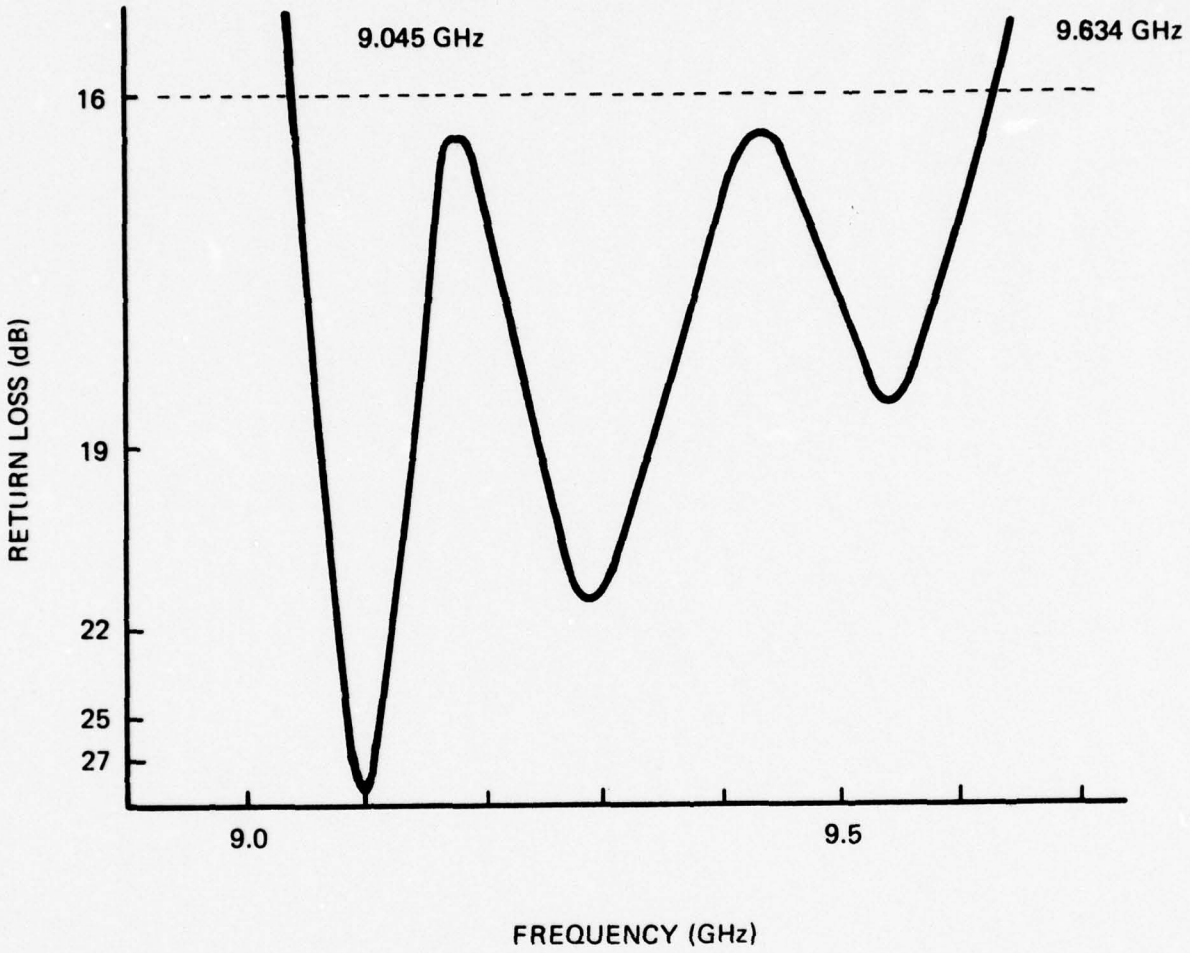


FIGURE 9 RETURN LOSS CHARACTERISTIC OF LIMITER INPUT FILTER

IV. FABRICATION OF BULK LIMITERS

A. High Resistivity Silicon Material

The quality of high resistivity uncompensated silicon material is probably the most important requirement for manufacturing high power and low insertion loss semiconductor bulk limiters. Very high resistivity uncompensated silicon cannot be grown by epitaxial processes. Thus, the use of epitaxial wafers in bulk limiter fabrication is ruled out and all processing must be accomplished using very thin float-zone refines silicon wafers. The important parameters that one must control are low crystalline defect density, controllable doping density, and precisely controllable wafer processing steps.

B. Wafer Dicing and Polishing

During the last quarter, a new source of high resistivity silicon ingot was used to fabricate the bulk limiters. The ingot was grown by the float zone method by Wacker Chemical Company, Munich, West Germany. It is ingot number W30736-6, resistivity 10.4 - 15.0 X 10^3 ohm/cm, <111> orientation, p type uncompensated with lifetime of 2 X 10^3 microseconds.

The ingot was mounted on a graphite block with epoxy resin. The wafers were then saw cut 10 mils thick on the <111> orientation on an STC (Silicon Technology Corporation, Oakland, NJ) inside diameter slicing machine. At this point in the as-sawn condition, maximum linear thickness variation was less than 0.4 mils and maximum bow was approximately less than 0.2 mils.

The wafers were then chemically etched to remove at least one mil of silicon from each side. An etching solution of modified 6:1:1 (HNO_3:HF:HAc) mixture was used, resulting wafers varying in thicknesses from 7.8 to 8.4 mils.

These wafers were separated in 0.1 mil thickness increments and mounted on stainless steel polishing blocks. One side was chemically-mechanically polished; the wafers were dismounted and solvent cleaned, then remounted for opposite side polishing. Optimum process conditions of slurry pH, hydraulic pressure, slurry temperature, and polishing time were utilized. A final double-sided wafer polishing thickness for two separate processing runs of 3.5 - 3.6 mils and 3.8 - 4.2 mils respectively, were obtained. Linear thickness variation of 0.2 mils maximum was obtained.

It appears that appropriate processing conditions for slicing, etching, cleaning, mounting, and polishing have been developed to obtain damage-free, very high resistivity, very thin silicon wafers, Further efforts will be made to establish the reproducibility of these processing parameters. This method produced a flatter wafer without sharp edges which permitted fabrication processes to proceed with lower breakage and consequently, improve yield.

C. Wafer Processing

During the last quarter, 16 high resistivity silicon wafers were processed for the fabrication of bulk limiters. First, silicon wafers were thinned down to 3.0 mil thickness by polishing and etching techniques. Then, the wafers were phosphorous diffused at 1000^{o}C for 30 minutes using $POCl_3$ diffusion system. After the completion of phosphorous diffusion, the phosphorous doped glass on the wafer was etched in hydrofluoric acid and 1000 Å of a silicon dioxide (SiO_2) glass was thermally grown at 1000^{o}C.

Both surfaces of the wafer were then photoprocessed in sequential operations which transfer the 0.75 mil checkerboard pattern of the photoresist mask to the silicon wafer. The checkerboard pattern windows were then etched through the SiO_2 and phosphorous doped silicon layers by using buffered hydrofluoric acid and 12:1:1 (HNO_3:HF:CH_3COOH) respectively. The wafer

was then diffused with boron at 950°C for 20 minutes using a boron nitride source. The boron diffused wafer was etched in hydrofluoric acid to remove all glass from the wafer surfaces.

Both surfaces of a wafer were then metallized with 500 - 1000 Å layer of chromium and 2000 - 3000 Å layer of gold and then electroplated with pure gold. One surface was plated to a thickness of 0.1 mil while the other was plated to a thickness of 4.0 mils. Then bulk limiter wafers were saw cut into 40 mil squares and were separated into individual chips.

After diffusion bonding with 8 mil diameter gold wire; the chips were mesa etched in silicon etch and passivated with silicon nitride and Dow Corning DC-643 junction coating. The bulk limiter chips were mounted in copper X-band irises and were tested for both low and high level RF performance. The typical DC characteristics of various runs and RF performance are given in Tables I, II, and III.

S/N	P_o (kW)	P_f (W)	P_s (W)	P_h (W)	R_T (μsec)
BL3B-2	2.1	100	310	100	2.0
BL3B-3	2.0	25	160	31	2.0
BL3B-4	2.0	25	140	50	2.0
BL3C-1	2.0	28	30	28	2.0
BL3C-2	1.0	31	160	31	1.8
BL3C-4	2.1	63	160	63	1.5
BL3C-5	2.0	50	160	50	1.5
BL4A-1	3.0	80	310	80	2.0
BL4A-2	1.0	B.O.			
BL4A-4	5	31	310	31	2.0

* Wafers procured from RRC International and processed at Microwave Associates

Test Conditions: $f = 9.6$ GHz, $t_p = 1.0$ μsec, $P_{rr} = 1000$ Hz, Crystal Calibration = 10 mW
(All limiters were tuned to $f_o = 9.6$ GHz)

TABLE I: High Power Test Data of Bulk Limiters of BL-3 and BL-4 Runs*

BULK LIMITER NO.	CAPACITANCE (pF)	RESISTANCE (k ohms) +
BL7A-1A	0.19	300
BL7A-1B	0.25	300
BL7A-1C	0.23	300
BL7A-1D	0.22	300
BL7A-1E	0.22	300
BL7A-1F	0.23	300

+ Zero bias at 1 MHz using Boonton Capacitance Bridge Model No. 75D.

* New high resistivity wafers completely processed at Microwave Associates.

TABLE II (a): DC Characteristics of Bulk Limiters from BL-7A Run*

SAMPLE NO.	CENTER FREQ. (MHz)	3 dB BANDWIDTH (MHz)	INSERTION LOSS (dB)
BL7A-1A	8850	530	1.3
BL7A-1-B	9700	620	1.3
BL7A-1-C	9600	630	0.9
BL7A-1-D	9530	710	1.0
BL7A-1-E	9150	550	1.0
BL7A-1-F	9600	710	0.9

TABLE II(b): Low Level Test Data Bulk Semiconductor Limiters

PROD. APPROVED	DATE 12-14-76	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 1

SPECIFICATION SCS-486 LOT SIZE SALES ORDER NO.

PARAMETERS	f_o	P_{IN}	R_T	P_{IN}	R_T
TEST CONDITIONS		t_p = 1.0 μsec PRR = 1x10³ Hz	@3.0db PT.	t_p = 1.0 μsec PRR = 1x10³ Hz FREQ. = 9.0 GHz	@3.0db PT
MIN. LIMITS					
MAX. LIMITS		30kw	.8 μsec		
	BULK LIMITER ONLY			BULK LIMITER IN PACKAGE	
S/N BL7A-1-A	8850	30kw	≈2.0 μs	30kw	≈2.0 μs
S/N BL7A-1-B	9170	15kw	1.75 μs	15kw	1.75 μs
S/N BL7A-1-C	9600	30kw	1.5 μs	30kw	1.5 μs
S/N BL7A-1-D	9530	30kw	1.5 μs	30kw	1.5 μs
S/N BL7A-1-E	9150	30kw	1.8 μs	30kw	1.8 μs
S/N BL7A-1-F	9600	30kw	1.6 μs	30kw	1.6 μs
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					

TABLE II(c): High Level Test Data Bulk Semiconductor Limiters in Single Slot X-Band Copper Irises

TESTED BY: DATE: Q. C. APPROVED BY: DATE:

FORM 707-C

S/N	f_o	3 dB Bandwidth	Li at f_o	P_o
BL-7A-A	9120 MHz	1.310 GHz	0.9 dB	27 kW (recovery time 1.5 μsec at 25 kW)
BL-7A-B	9170 MHz	1.510 GHz	0.6 dB	18 kW
BL-7A-C	9200 MHz	1.800 GHz	0.5 dB	Accidently BO
BL-7A-D1	9600 MHz	1.370 GHz	0.4 dB	20 kW

TABLE III: Test Data on Double Slot Limiters

V. FABRICATION AND RF TESTING OF THE BULK DIODE LIMITER ASSEMBLY

A. Bulk Limiter Tuning

The bulk diode limiter assembly consists of the bulk limiter followed by a two stage diode clean up limiter. In combining the bulk limiter with the diode limiter for the First Engineering Samples, it was necessary to use tuning screws in front and back of the bulk limiter to achieve optimal bandwidth performance. But this had an adverse effect on the peak power handling capability of the bulk diode limiter assembly as shown in Tables IV and V. The peak power handling capability was reduced approximately by a factor of two.

B. Matching Structure Optimization and RF Testing of the Bulk Diode Limiter Assembly

1. Single Slot Results

A new matching structure was investigated in which all tuning was accomplished with elements between the bulk limiter and clean up limiter and is discussed in detail in Section III. This design retains the power handling performance of the bulk stage combined with clean up stage as shown in Table II(c). A bulk limiter element mounted in a single slot X-band copper iris is shown in Fig. 10 and typical low level RF performance is shown in Fig. 11. But because the circuit tested was not optimized for bandwidth and the theoretical design required for broader bandwidth bulk limiters, only narrow band performance was achieved. Two bulk limiters were mounted in double slot iris to increase the bandwidth.

2. Double Slot Results

Bulk limiter elements from BL7A run were also mounted in X-band double slot irises. A bulk limiter element mounted in a double slot iris is shown in Fig. 12 and low level RF performance is shown in Fig. 13.

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 2

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	Li	VSWR		Po Note 1	Pf	Ps	Pb	ts		Po Note 1	Pf	Ps	Pb	ts
TEST CONDITIONS	9.0GHz 9.65	9.0GHz 9.65		Frequency - 9.0GHz tp = 1μs, Prr = 1 x 10^3 Du = .001						Frequency - 9.3GHz tp = 1.0 μs, Prr = 1 x 10^3 DU = .001				
MIN. LIMITS	—	—		—	—	—	—	—		—	—	—	—	—
MAX. LIMITS	0.7dB	1.4:1		30kw	50mw	.75w	—	—		30kw	50mw	.75w	—	—
PACKAGE:	BULK LIMITER WITH CLEAN-UP LIMITER													
S/N 1-30R	1.1	1.46		15kw	50mw	1.6w	25mw	8ns		8kw	20mw	1.0w	31mw	5ns
S/N														
S/N 1-6	.9	1.48		9kw	60mw	1.6w	60mw	8ns		7kw	<10mw	1.0w	30mw	6ns
S/N														
S/N 1-10-7	1.0	1.35		10kw	50mw	1.6w	50mw	8ns		8kw	<10mw	5w	31mw	5ns
S/N														
S/N														
S/N 1-BL-3-2	.9	1.58		MICROWAVE ASSOCIATES SEMICONDUCTOR MATERIAL										
S/N 1-BL-3-3	1.1	1.7		MICROWAVE ASSOCIATES SEMICONDUCTOR MATERIAL										
S/N														
S/N				NOTE 1. IN ALL CASES Po WAS DETERMINED WHEN THE RECOVERY TIME REACHED										
S/N				2.0 μsec AT THE 3.0 dB POINT.										
S/N														
S/N														
S/N														
S/N														

TABLE IV LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITH CLEAN UP LIMITER

TESTED BY: DATE: Q. C. APPROVED BY: DATE:

FORM 707-C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS - 3940XM	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 2

SPECIFICATION SCS-486 LOT SIZE 5 SALES ORDER NO.

PARAMETERS	Po Note 1	Pf	Ps	Pb	ts
TEST CONDITIONS	Frequency - 9.6GHz tp = 1.0 μs Prr = 1 x 10^3 Du = .001				
MIN. LIMITS	—	—	—	—	—
MAX. LIMITS	30kw	50mw	.75w	—	—
PACKAGE:	BULK LIMITER WITH CLEAN-UP LIMITER				
S/N 1-30R	10kw	<10mw	.5w	20mw	5ns
S/N					
S/N 1-6	10kw	<10mw	.5w	16mw	5ns
S/N					
S/N 1-10-7	9kw	<10mw	.5w	16mw	5ns
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					
S/N					

NOTE 1. IN ALL CASES Po WAS DETERMINED WHEN THE RECOVERY TIME REACHED 2.0 μsec AT THE 3.0 dB POINT

TABLE IV(a) LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITH CLEAN UP LIMITER

TESTED BY: _____ DATE: _____ Q. C. APPROVED BY: _____ DATE: _____

FORM 707-C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS -	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 1	OF 2

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	Li	f_o	B.W. @3 dB	P_o (1)	P_f	P_s	P_b	t_s
TEST CONDITIONS	f_o			Frequency -9.0 GHz, t_p = 1 μsec, Prr = 1 X 10^3 Hz, Du = .001				
MIN. LIMITS	---	---	---	---	---	---	---	---
MAX. LIMITS	---	---	---	---	---	---	---	---
BULK LIMITER ALONE								
S/N 30R	1.4dB	9.20GHz	.670 GHz	15kW	40 W	100W	40 W	20ms
S/N								
S/N 6	.8dB	9.16 GHz	.850 GHz	13kW	40 W	160 W	60W	20 ms
S/N								
S/N 10-7	1.8 dB	9.15 GHz	.930 GHz	15kW	40 W	130 W	60 W	20 ms
S/N								
S/N								
S/N BL-3-2	1.0	9.30 GHz	1.010 GHz					
S/N BL-3-3	1.6	9.10 GHz	.770 GHz					
S/N								
S/N								
S/N								
S/N	NOTE: (1) IN ALL CASES P_o WAS DETERMINED WHEN THE RECOVERY TIME REACHED 2.0 μsec AT THE 3.0 dB POINT.							
S/N								
S/N								
S/N								

TABLE V LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITHOUT CLEAN UP LIMITER

TESTED BY: _____ DATE: _____ Q. C. APPROVED BY: _____ DATE: _____

FORM 707-C

PROD. APPROVED	DATE	MICROWAVE ASSOCIATES, INC.	DS -	ISSUE
Q. C. APPROVED	DATE	TEST DATA SHEET	SHEET 2	OF 2

SPECIFICATION _____ LOT SIZE _____ SALES ORDER NO. _____

PARAMETERS	(1) P_o	P_f	P_s	P_b	t_s		(1) P_o	P_f	P_s	P_b	t_s				
TEST CONDITIONS	FREQUENCY - 9.3 GHz t_p = 1.0 μsec, Prr = 1 X 10^5 Hz Du = .001						FREQUENCY - 9.6 GHz t_p = 1 μsec, Prr = 1 X 10^3 Hz Du = .001								
MIN. LIMITS	---	---	---	---	---		---	---	---	---	---				
MAX. LIMITS	---	---	---	---	---		---	---	---	---	---				
BULK LIMITER ALONE															
S/N 30R	20 kW	16 W	100W	16 W	10 ms		15 kW	25W	100W	50W	20 ms				
S/N															
S/N 6	17kW	40W	100W	40W	20 ms		15 kW	20W	130 W	31 W	20 ms				
S/N															
S/N 10-7	15kW	25 W	100W	25 W	20 ms		15 kW	25 W	100 W	40 W	20 ms				
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															
S/N															

NOTE: (1) IN ALL CASES P_o WAS DETERMINED WHEN THE RECOVERY TIME REACHED 2.0 μsec AT THE 3.0 dB POINT.

TABLE V LOW AND HIGH POWER TEST RESULTS OF FIRST ENGINEERING SAMPLES WITHOUT CLEAN UP LIMITER

TESTED BY: _____ DATE: _____ Q. C. APPROVED BY: _____ DATE: _____

FORM 707-C

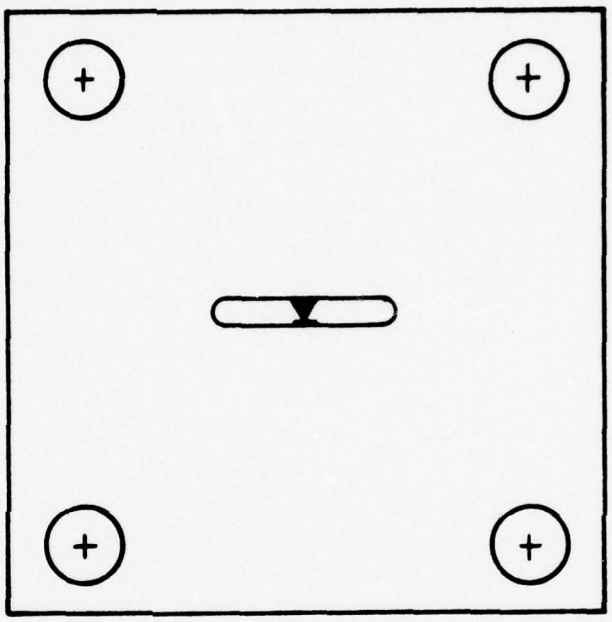
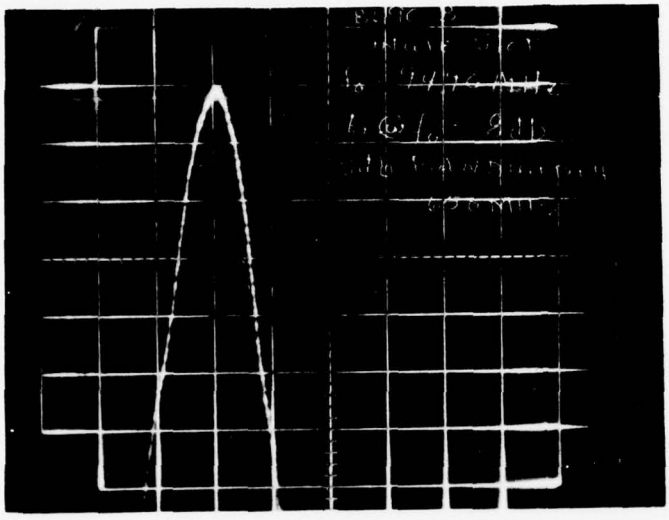


FIGURE 10 SINGLE SLOT BULK LIMITER



BL9C - 3

SINGLE SLOT

f_o = 9.49 GHz

Li @ f_o = 0.8 dB

BANDWIDTH (3dB) = 0.650 GHz

FIGURE 11 LOW LEVEL RF PERFORMANCE OF SINGLE SLOT BULK LIMITER

N-15456

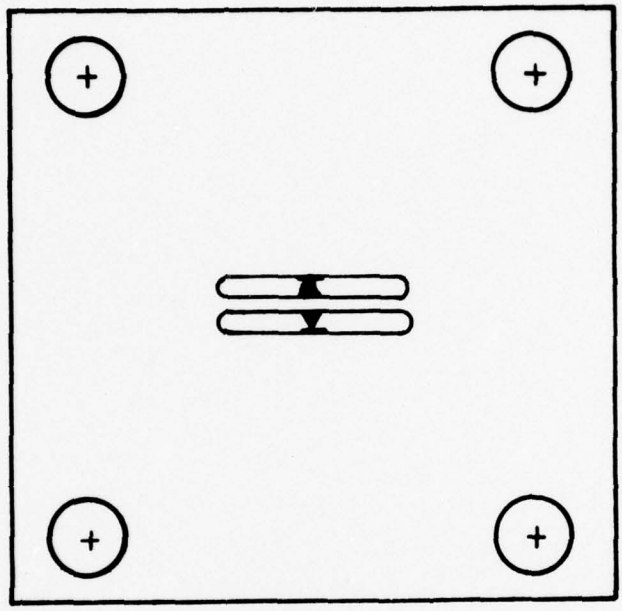
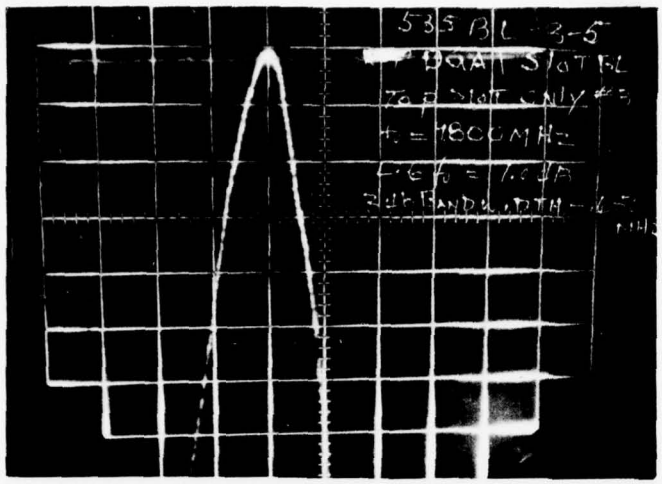


FIGURE 12 DUAL SLOT BULK LIMITER



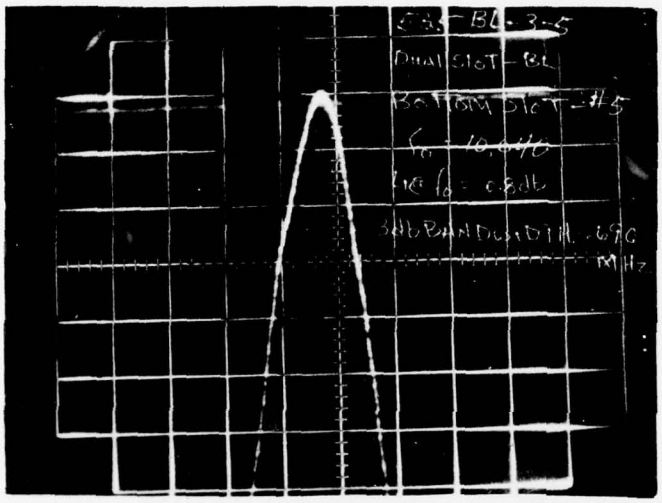
535 BL-3-5

TOP SLOT #3

A. f_o = 9.8 GHz

Li @ f_o = 1.0 dB

BANDWIDTH (3dB) = 0.650 GHz

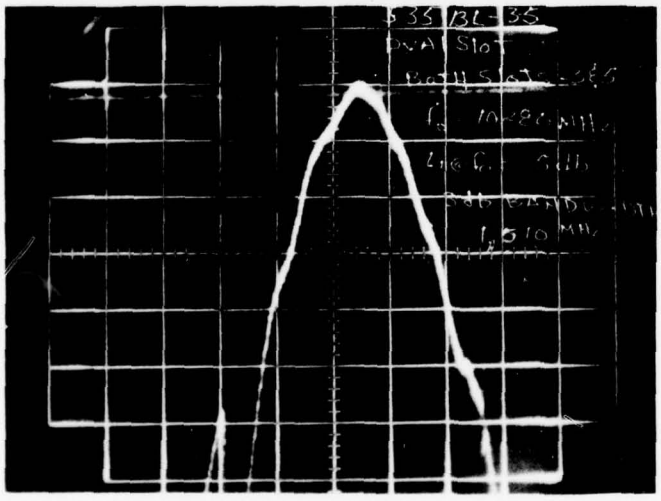


BOTTOM SLOT #5

B. f_o = 10.04 GHz

Li @ f_o = 0.8 dB

BANDWIDTH (3dB) = 0.690 GHz



DUAL SLOT -- 3 & 5

C. f_o = 10.280 GHz

Li @ f_o = 0.5 dB

BANDWIDTH (3dB) = 1.510 GHz

FIGURE 13 LOW LEVEL RF PERFORMANCE OF DUAL SLOT BULK LIMITER

N-15457

Figures 13 (a) and 13 (b) show insertion loss and 3 dB bandwidth of individual slots which were measured by shorting the other slot by metallic tape. Dual slot results are given in Fig. 13 (c) and show that 3 dB bandwidth of 1.51 GHz was achieved. Low level and high power performance of typical bulk limiters in dual slot irises is shown in Table III. This test data shows that the dual slot configuration exhibits wider bandwidth and is capable of handling peak RF power of 18 kW to 27 kW.

In the single slot case, the degradation in recovery time above 2 μsec generally indicates that the diode is heating up and will burnout with a further increase in RF power. No such correlation was observed in dual slot units, which makes it difficult to test the unit to peak power performance without destruction.

3. Recovery Time vs RF Power

The recovery time of bulk limiters from BL 7A run was measured in the dual slot iris versus RF power. Single slot measurements were also made on the same unit by shorting one slot with metallic tape. The results are given in Fig. 14 and show reduced recovery time for the dual slot limiter.

4. Recovery Time vs Temperature

A single slot bulk limiter from BL 7A was subjected to a cold test in the following manner: (1) at room temperature, the input power to the device was set at 11.8 kW with resulting recovery time of 1.5 μsec, (2) the device was then enclosed in a box filled with dry ice; the recovery time was decreased to 1.1 μsec and (3) the input power was then increased to bring the recovery time to 1.5 μsec which occured at 17.8 kW. This shows that device cooling is important in obtaining high power and short recovery time device performance.

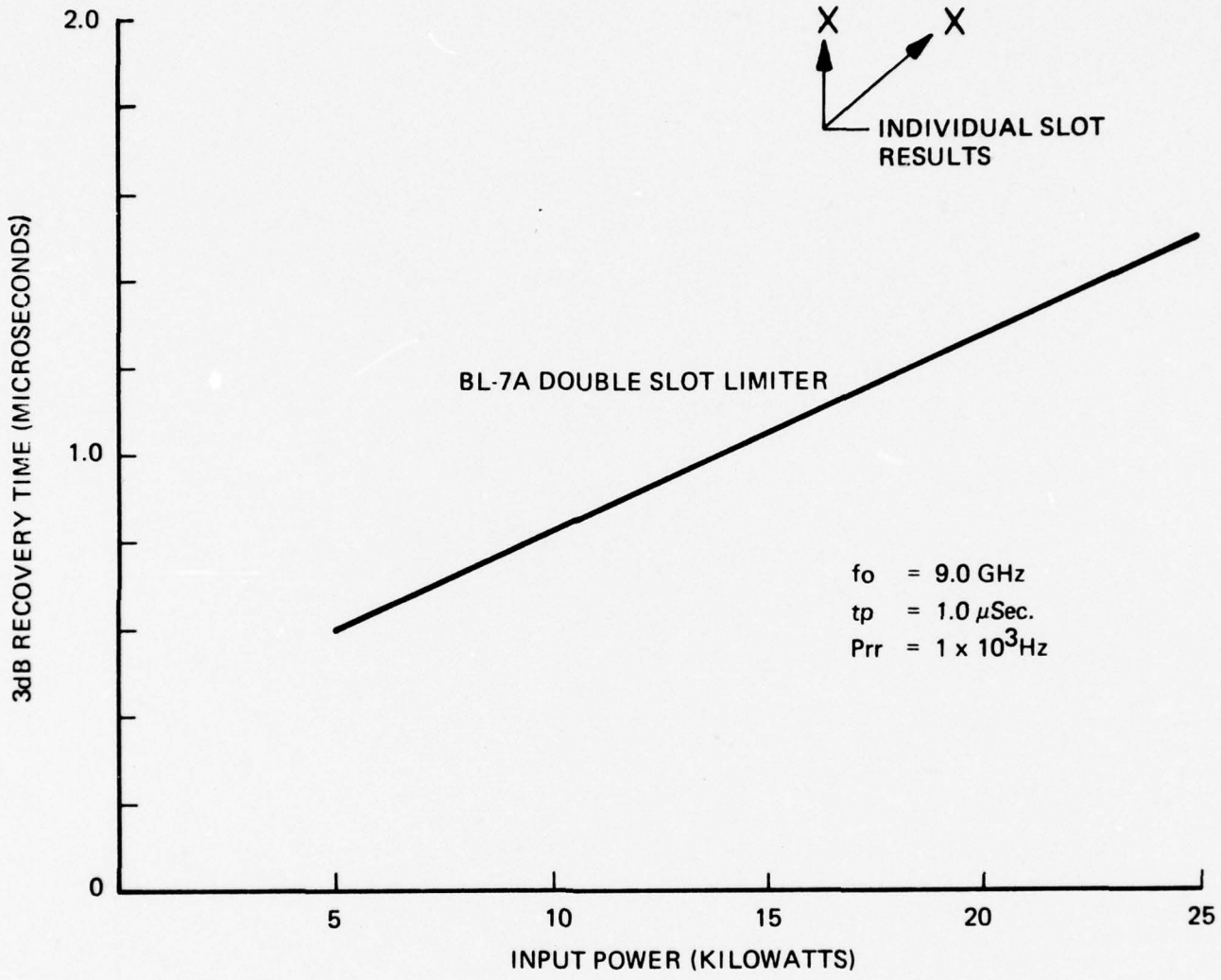


FIGURE 14 RECOVERY TIME VS INPUT RF POWER

D-15462

VI. PROBLEM AREAS

A. Batch Process

In order to improve the manufacturability of bulk limiters, a batch fabrication scheme is under development. This will eliminate the delicate diffusion bonding which is currently in use. Presently we are having problems in the photo plating process which will be resolved in the next quarter.

B. Metallization

Difficulties have been encountered in depositing reproducible evaporated chrome gold films. Other schemes such as electron beam evaporation and sputtered Cr-Au films are under investigation to improve adhesion.

C. Dual Slot Failure Mechanism

A problem has been encountered in predicting burnout of dual slot bulk limiters from recovery time measurements. Typically, single slot units do not burnout until recovery time exceeds 2 microseconds. No such pre burnout indication was found with dual slot units.

D. Recovery Time

The recovery times obtained with both single and dual slot bulk limiters have been in the order of 1.5 to 2 microseconds. This may be reduced by geometry changes being incorporated in the batch fabrication work currently underway.

VII. DELIVERIES

During the quarter, we delivered First Engineering Sample diodes (Item 0001AA) to the U. S. Army Electronics Command. These included five (5) X-band semiconductor bulk limiters and a clean up limiter. The electrical test data of these diodes is given in Table IV.

VIII. CONCLUSIONS

X-band bulk limiters have been fabricated using a new high resistivity silicon with $\rho = 10.4 - 15.0 \times 10^3$ ohm cm (p type) with lifetime of 2×10^3 microsecond. Improvements in polishing, lapping, and photolithographic processing were implemented which improved wafer yield considerably. During the second quarter a number of wafers were produced with the low impedance DC characteristics necessary for high power microwave performance.

The interaction of broadband tuning techniques on power handling capability was examined. A new circuit was developed and successfully tested with bulk limiters fabricated during the second quarter. Bulk limiter performance requirements to meet package performance goals were calculated from test results.

Bulk limiters were fabricated using single and double slot copper X-band irises. Power handling capabilities of 20 kW to 30 kW were observed at a recovery time of 2.0 microseconds. Dual slot bulk limiters exhibited improved bandwidth as predicted by design analysis.

IX. PROGRAM FOR THE NEXT QUARTER

During the next quarter, we will fabricate devices with improved yield and performance by a batch process which will eliminate the gold wire diffusion bond to the bulk limiter element. High temperature metallization (Ti-W-Au) and low temperature glass passivation schemes will be implemented to further improve the power handling capability of the bulk limiters.

We have received high resistivity silicon material <111> orientation grown by Hughes Aircraft through USAECOM for bulk limiter evaluation in the next quarter.

X. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program.

TITLE	HOURS
Project Manager	325
Silicon Materials Manager	25
Senior Processing Engineer	30
Processing Engineer	60
Limiter Engineer	85
Engineering Assistant (Fabrication)	500
Engineering Assistant (Test)	200

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts

MIL-STD-1311A Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1 μsec pulses continuous	:	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss	:	0.7dB (max)
(c)	Low Level VSWR	:	1.4:1 (max)
(d)	Recovery Time	:	0.8 μsec (max)
(e)	Flat Leakage	:	50 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(f)	Spike Leakage	:	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias	:	none

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (QCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance Inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

4.6 Test Conditions

Parameter Unit	T_A °C	Fo GHZ	Po Watts	μsec	P_{RR} Pulses/sec	Du	Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 - 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μ sec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformance Inspection - Part 1 (QC 1-1)

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	No.
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_L Δf_3 $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_L Δf_3 $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_L Δf_3 $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_L Δf_3 $\Delta \tau$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_i		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	γ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC111-3)

The maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

A swept frequency may be used.

Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a db increase of limiter insertion loss compared to the "cold" insertion loss.

Quality conformance test to be made using bulk semiconductor stage only.

For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

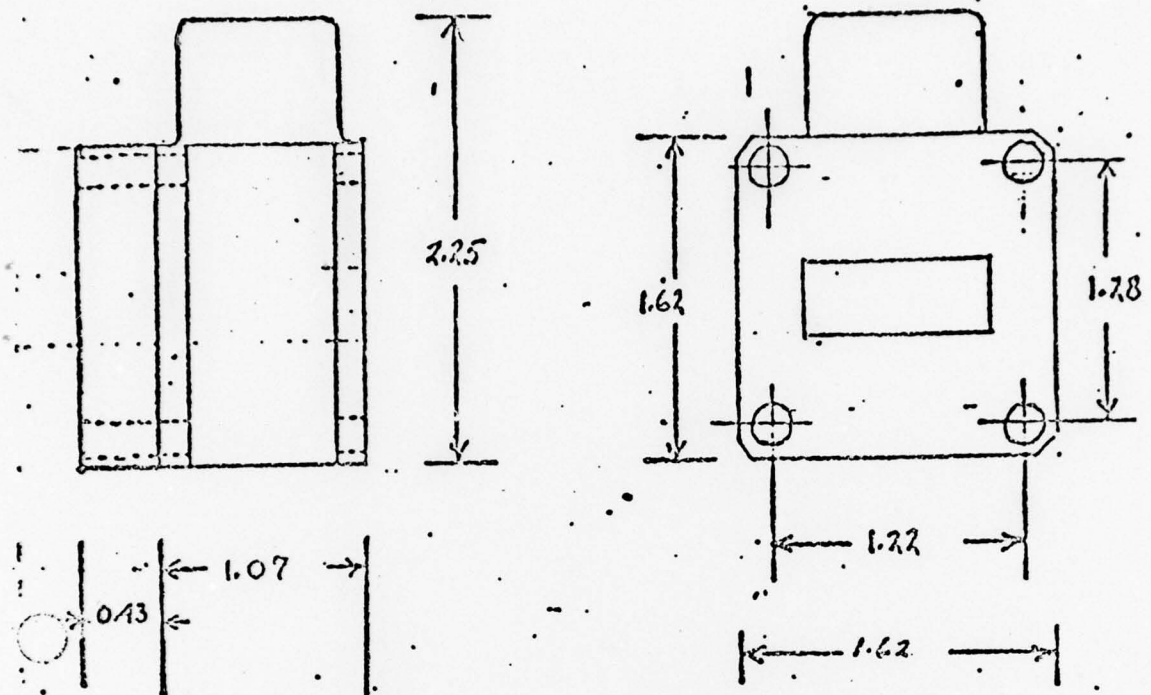
Measurement of parameters cited will follow the procedures outlined in QCI -1.

The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage $(P_s)_1$ will be periodically monitored. Life test will be interrupted each 720 ± 20 hours intervals to permit testing of end of life test end points.

5. PREPARATION FOR DELIVERY

5.1 Packaging, Packing and Marking. - Packaging, packing and package marking shall be specified in the contract.

LINE DRAWING



Notes:

a) all dimensions in inches

b) all tolerances ± 0.05 unless otherwise specified

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